SD/MMC Interface Integration Guidelines

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SD/MMC cards provide a low cost solution for data logging and storage applications for embedded systems. SD/MMC cards can be easily interfaced with a Microcontroller using an SPI interface and between one and three control lines. While the electrical interface is relatively straight forward, successfully implementing a solution can be time consuming for the initial implementation. This document looks at some of the common pitfalls encountered. The document assumes the developer is implementing Brush Electronics SD/MMC File System drivers or Utilities with a Microchip PIC Microcontroller however the principles apply to other implementations.

For developers that are implementing an SD/MMC interface for the first time, we recommend using our SD/MMC Card driver and test utilities software (http://www.brushelectronics.com/index.php?page=software#SDUTIL) for bringing up new hardware and gain familiarity with the SD/MMC integration before moving on to implementing a File System.

Troubleshooting guidelines are split into three different areas:

- Power Supply
- SPI BUS
- Media

Power Supply

SD/MMC cards provide a relatively low power storage solution for embedded controllers however implementers often do not pay enough attention to the peak power requirements and inrush currents and may encounter situations where the embedded system resets when an SD/MMC card is inserted or the SD/MMC card may stop talking to the Microcontroller.

The power supply circuitry must be able to deal with the momentary inrush current when a card is inserted. This inrush current can be of the order of 200mA. Generally this is handled using large value power supply filter capacitors before and after the voltage regulator. Ignoring the requirements for other components of an embedded system, typical values for the power supply input capacitor are in the range of 220uF to 470uF. Lower value capacitors than have low ESR (Effective Series Resistance) could be use used. A typical value for the filter capacitor after the regulator is 47uF tantalum capacitor.

In situations where the SD/MMC card socket is not located in close proximity to the regulator filter capacitors, an additional 22uF tantalum capacitor should be placed as close as practical to the SD/MMC card socket between pins 3 and 4 of the socket.

A 100nF power supply decoupling capacitor should be placed as close as practical to the SD/MMC card socket between pins 3 and 4 of the socket.

SPI Bus

The SPI bus interface between the Microcontroller and the SD/MMC card is straight forward however it is the area that causes the most problems for first time implementers. The interface includes the following mandatory signals.

Microcontroller		**SD/MMC Card**	
SDI	(input)	DO	(output)
SDO	(output)	DI	(input)
SCK	(output)	SCK	(input)
CS	(output)	CS	(input)

The Microcontrollers SPI hardware interface drives the SDI, SDO and SCK control lines. The CS line from the PIC is an I/O pin configured as an output that provides the active low chip select input of the SD/MMC card.

Two optional control lines from the SD/MMC card to the Microcontroller are the CD (Card detect) and WP (Write protect) switch outputs. By convention, these outputs are active low.

In dual voltage systems where the Microcontroller runs at a different supply voltage to the SD/MMC card, level conversion logic is required between the Microcontroller and the SD/MMC cards. There are multiple ways of implementing level conversion. The following link gives an example using a pair of 74ACT125M transceivers to perform the level conversion: http://www.ljcv.net/picnet1/picnet1-ds0.pdf Here is another example using a single transceiver combined with resistors: http://www.brushelectronics.com/download/BE_Reference_Design_PIC18F4620_ENC28J60.zip

The SPI bus must be correctly terminated. The SDI, CS, CD and WP lines all require pull-up resistors in the range of 10K to 100K. A common omission is the pull-up resistor on the SDI line which will result in intermittent problems with the SD/MMC initialisation sequence.

The SPI BUS frequency should in principle be less than or equal to 400KHz for the initialisation phase of the card and then can ramped up to 20MHz for subsequent operation. Operating the SPI bus beyond 20MHz can result in read/write errors.

The SPI bus is often a shared system resource. An SPI bus conflict occurs when two or more chip select lines to peripherals sharing the SPI bus are asserted concurrently. This can result in read / write errors and can result in an SPI device isolating itself

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from the SPI bus. SPI bus conflicts is a common first time implementation problem which typically occurs when bringing up a new system during development.

Media Format

The Brush Electronic SD/MMC File System Drivers and the Utilities software interpret the data structures that are present on the SD/MMC card. For a card to be used with this software, the card must be formatted on a system such as a PC or a Camera.

During the format process, some operating systems examine the data structure that exist on a card and format the card based on the existing structures. In rare situations it is possible that the master boot record containing a partition table structure is corrupt and is not correctly dealt with by the format programs. In this event the Brush Electronics software may not be able to correctly interpret and file system structure and a file system read error may result. If this occurs, format the media with a device that does not generate a partition table, such as a digit camera.

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